

Spread Spectrum Clock Generator MB88153A

MB88153A-100/101/110/111

■ DESCRIPTION

MB88153A is a clock generator for EMI (Electro Magnetic Interference) reduction. The peak of unnecessary (EMI) can be attenuated by making the oscillation frequency slightly modulate periodically with the internal modulator. It corresponds to both of the center spread which modulates input frequency as Middle Centered and down spread which modulates so as not to exceed input frequency.

■ FEATURE

- Power down pin : 10 μ A (Typ-sample) consumption current at power down
- Input frequency : 16.6 MHz to 134 MHz
- Output frequency : 16.6 MHz to 134 MHz (One-fold input frequency)
- Modulation rate can select from $\pm 0.5\%$, $\pm 1.5\%$ – 1.0% or – 3.0%. (For center spread / down spread.)
- Modulation clock output Duty : 40% to 60%
- Modulation clock Cycle-Cycle Jitter : Less than 100 ps
- Low current consumption by CMOS process : 4.0 mA (24 MHz : Typ-sample, no load)
- Power supply voltage : 3.3 V \pm 0.3 V
- Operating temperature : – 40 °C to +85 °C
- Package : 8-pin SOP

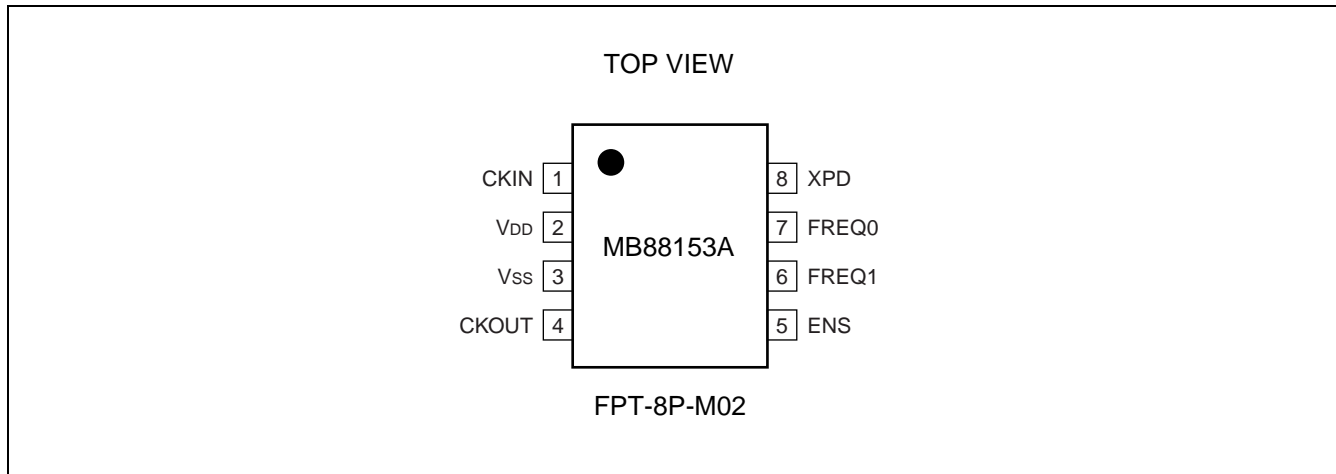
MB88153A

■ PRODUCT LINEUP

MB88153A has four kinds of modulation rate and modulation type (center spread/down spread).

Product	Modulation rate	Modulation type
MB88153A-100	-1.0%	Down spread
MB88153A-101	-3.0%	
MB88153A-110	±0.5%	Center spread
MB88153A-111	±1.5%	

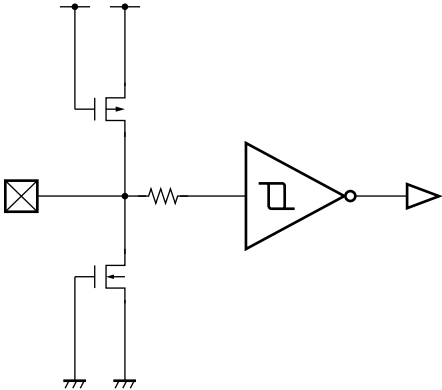
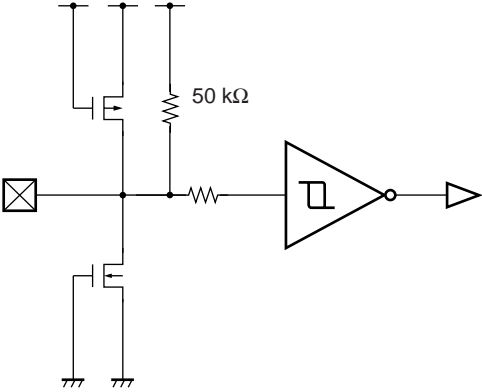
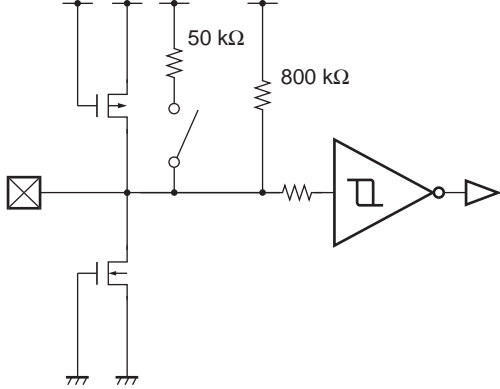
■ PIN ASSIGNMENT



■ PIN DESCRIPTION

Pin name	I/O	Pin no.	Description
CKIN	I	1	Clock input pin
V _{DD}	—	2	Power supply voltage pin
V _{SS}	—	3	GND pin
CKOUT	O	4	Modulated clock output pin “L” output at power down
ENS	I	5	Modulation enable setting pin
FREQ1	I	6	Frequency setting pin
FREQ0	I	7	Frequency setting pin (with pull-up resistor)
XPD	I	8	Power down pin (with pull-up resistor) Power down at “L” input

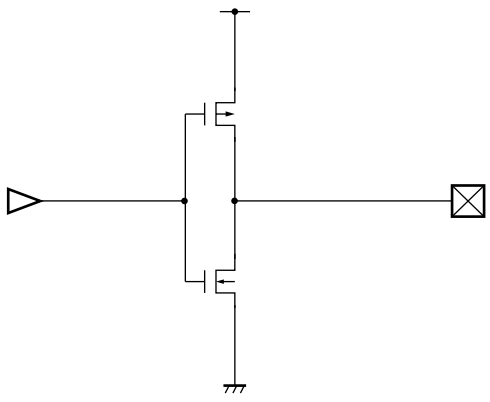
■ I/O CIRCUIT TYPE

Pin	Circuit type	Remarks
CKIN, ENS, FREQ1		CMOS hysteresis input
FREQ0		CMOS hysteresis input with pull-up resistor 50 kΩ (Typ)
XPD		CMOS hysteresis input with 50 kΩ + 800 kΩ (Typ) pull-up resistors Note : If "L" is input to XPD when the XPD function is selected, 50 kΩ pull-up resistor is disconnected.

(Continued)

MB88153A

(Continued)

Pin	Circuit type	Remarks
CKOUT	 <p>The diagram shows a CMOS output stage. An inverter symbol (a triangle with a small circle at its tip) is connected to the input of a CMOS inverter. The CMOS inverter consists of a PMOS transistor (top) and an NMOS transistor (bottom). The PMOS transistor's gate is connected to the input, and its source is connected to a power supply rail (indicated by a horizontal line with a vertical line extending upwards). The NMOS transistor's gate is also connected to the input, and its source is connected to a ground symbol (indicated by a horizontal line with two diagonal lines extending downwards). The output of the CMOS inverter is connected to a square symbol with an 'X' inside, representing the CKOUT pin.</p>	<ul style="list-style-type: none">• CMOS output• "L" output at power down

■ HANDLING DEVICES

Preventing Latch-up

A latch-up can occur if, on this device, (a) a voltage higher than V_{DD} or a voltage lower than V_{SS} is applied to an input or output pin or (b) a voltage higher than the rating is applied between V_{DD} pin and V_{SS} pin. The latch-up, if it occurs, significantly increases the power supply current and may cause thermal destruction of an element. When you use this device, be very careful not to exceed the maximum rating.

Handling unused pins

Do not leave an unused input pin open, since it may cause a malfunction. Handle by, using a pull-up or pull-down resistor.

Unused output pin should be opened.

Power supply pins

Please design connecting the power supply pin of this device by as low impedance as possible from the current supply source.

We recommend connecting electrolytic capacitor (about 10 μF) and the ceramic capacitor (about 0.01 μF) in parallel between V_{SS} pin and V_{DD} pin near the device, as a bypass capacitor.

Clock I/O circuit

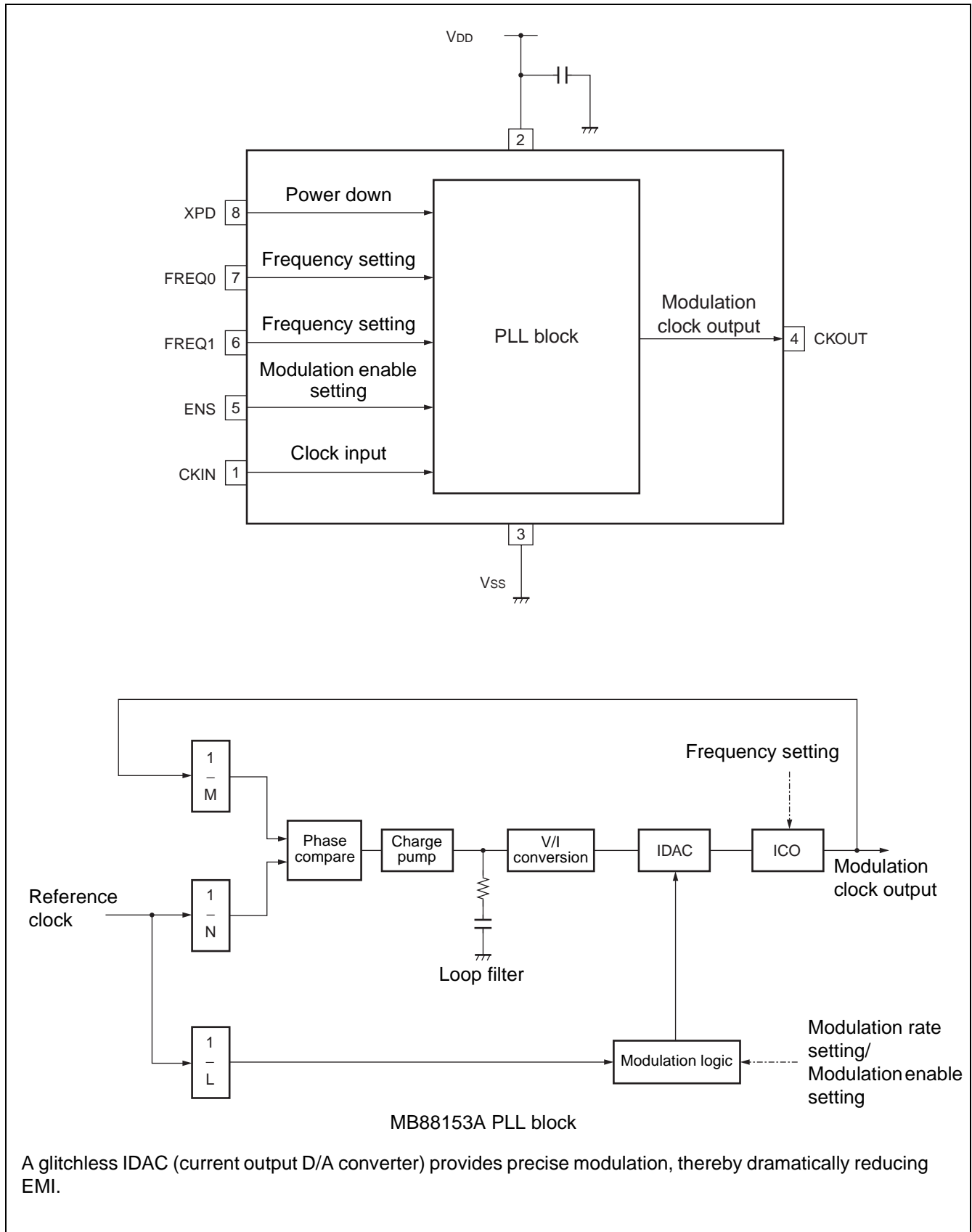
Noise near the CKIN pin may cause the device to malfunction. Design the printed circuit board so that the wiring for the clock input does not intersect any other wiring.

Please pay attention so that an overshoot and an undershoot do not occur to an input clock of CKIN pin.

Design the printed circuit board that surrounds the CKIN and CKOUT pins with ground.

MB88153A

■ BLOCK DIAGRAM



■ PIN SETTING

When changing the pin setting, the stabilization wait time for the modulation clock required. The stabilization wait time for the modulation clock takes the maximum value of Lock-Up time in “■ ELECTRICAL CHARACTERISTICS • AC Characteristics”.

ENS modulation enable setting

ENS	Modulation
L	No modulation
H	Modulation

Note : Spectrum does not spread when “L” is set to ENS. The clock with low jitter can be obtained.

FREQ0, FREQ1 frequency setting

FREQ0	FREQ1	Input frequency range
L	L	16.6 MHz to 40 MHz
L	H	66 MHz to 134 MHz
H	L	33 MHz to 67 MHz
H	H	40 MHz to 80 MHz

Note : It is set according to the frequency of the clock input to the device. Set FREQ0 pin to “H” for the pin opened because FREQ0 pin has pull-up resistor.

XPD power down setting

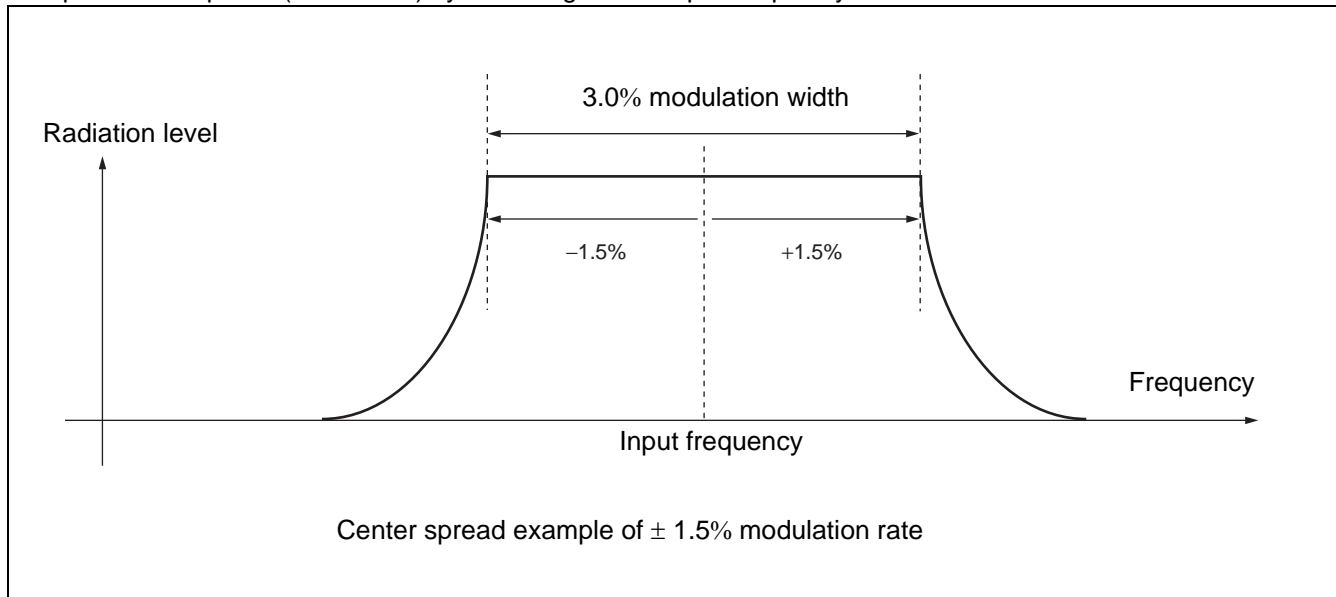
XPD	Power down
L	Power down
H	Normal operation

Note : When “L” is set to XPD pin, the power down operation is implemented and “L” is output to CKOUT pin. When “H” is input to XPD pin or XPD pin is opened, normal operation is implemented because the XPD pin has pull-up resistor.

MB88153A

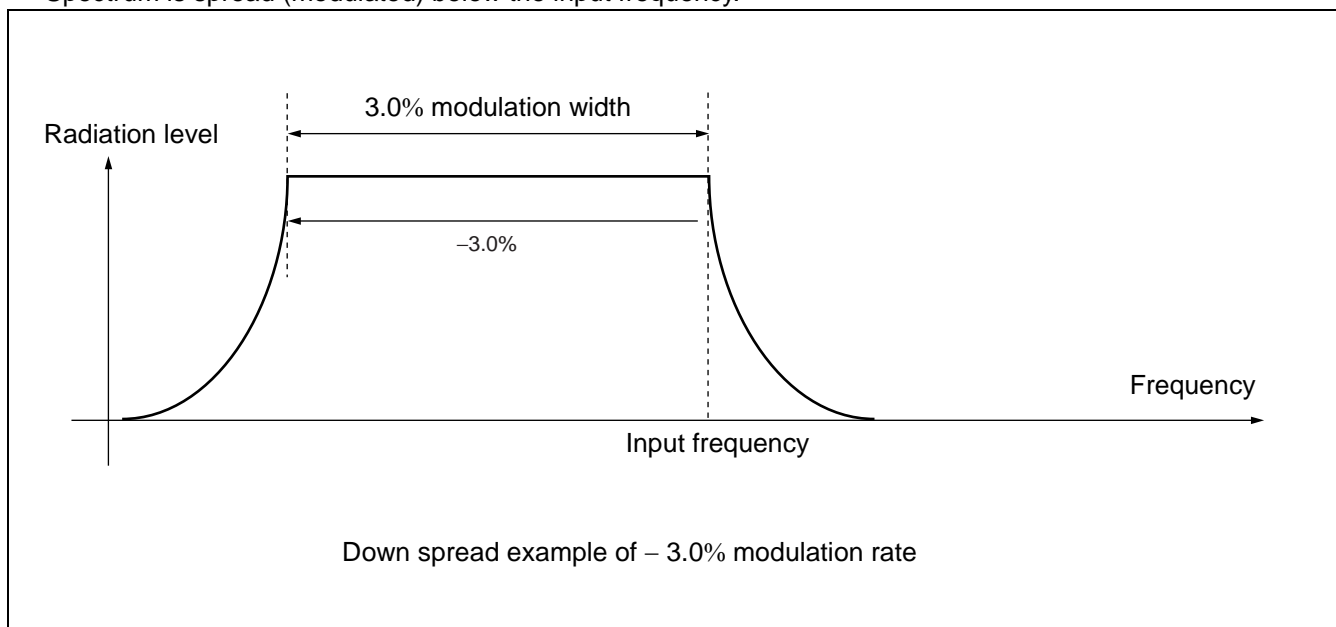
- Center spread

Spectrum is spread (modulated) by centering on the input frequency.



- Down spread

Spectrum is spread (modulated) below the input frequency.

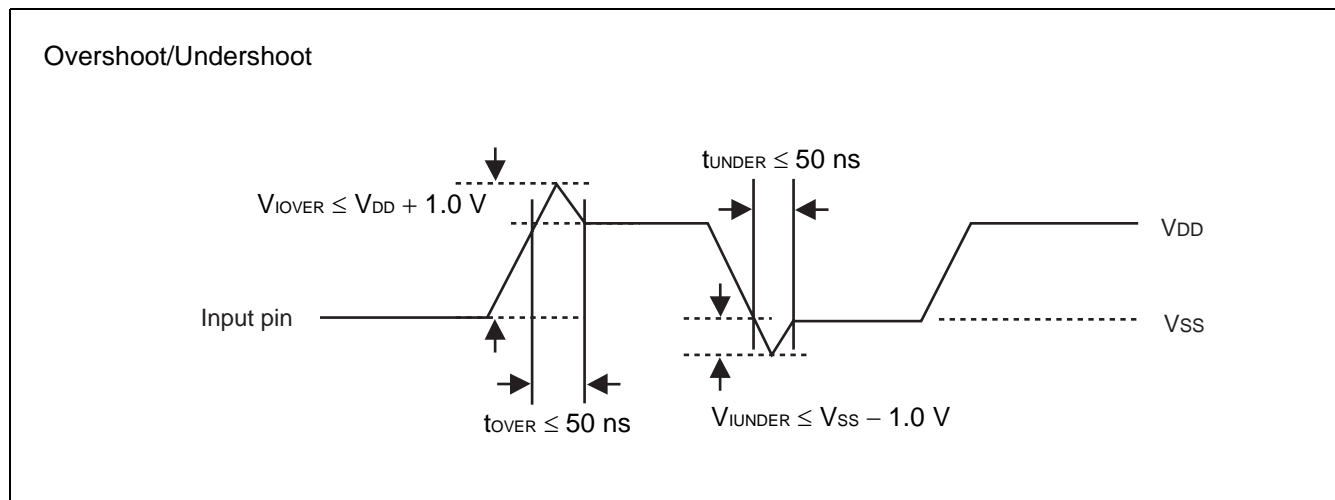


■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power supply voltage*	V_{DD}	- 0.5	+ 4.0	V
Input voltage*	V_i	$V_{SS} - 0.5$	$V_{DD} + 0.5$	V
Output voltage*	V_o	$V_{SS} - 0.5$	$V_{DD} + 0.5$	V
Storage temperature	T_{ST}	- 55	+ 125	°C
Operation junction temperature	T_J	- 40	+ 125	°C
Output current	I_o	- 14	+ 14	mA
Overshoot	V_{IOVER}	—	$V_{DD} + 1.0$ ($t_{OVER} \leq 50$ ns)	V
Undershoot	V_{IUNDER}	$V_{SS} - 1.0$ ($t_{UNDER} \leq 50$ ns)	—	V

* : The parameter is based on $V_{SS} = 0.0$ V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.



RECOMMENDED OPERATING CONDITIONS

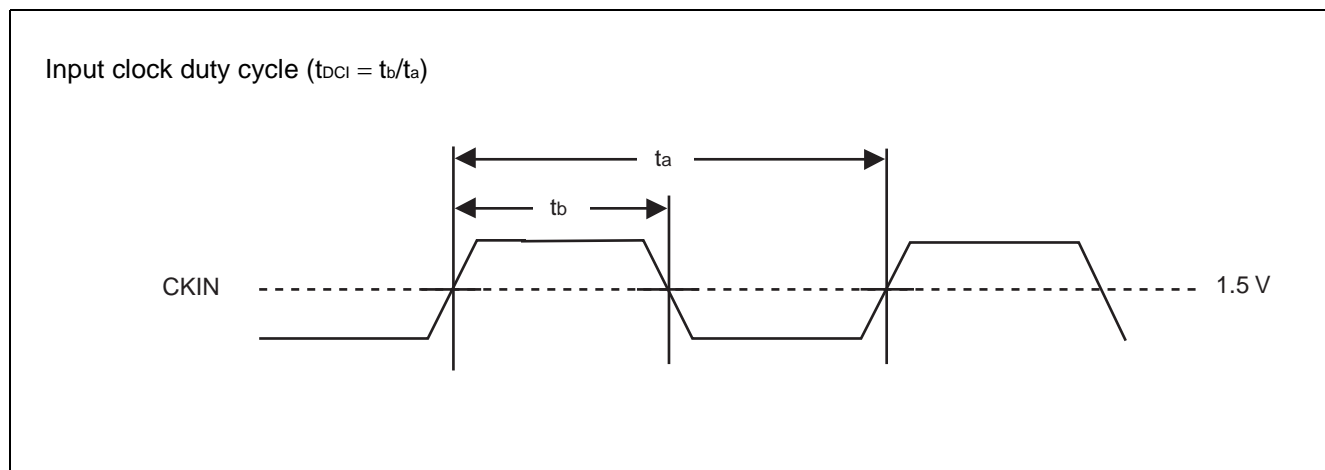
(V_{SS} = 0.0 V)

Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
Power supply voltage	V _{DD}	V _{DD}	—	3.0	3.3	3.6	V
“H” level input voltage	V _{IH}	CKIN, ENS, FREQ0, FREQ1, XPD	—	V _{DD} × 0.8	—	V _{DD} + 0.3	V
“L” level input voltage	V _{IL}	CKIN, ENS, FREQ0, FREQ1, XPD	—	V _{SS}	—	V _{DD} × 0.2	V
Input clock duty cycle	t _{DCI}	CKIN	16.6 MHz to 134 MHz	40	50	60	%
Operating temperature	T _a	—	—	− 40	—	+ 85	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device’s electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.



■ ELECTRICAL CHARACTERISTICS

• DC Characteristics

($T_a = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$, $V_{DD} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{SS} = 0.0\text{ V}$)

Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
Output voltage	V_{OH}	CKOUT	"H" level output $I_{OH} = -4\text{ mA}$	$V_{DD} - 0.5$	—	V_{DD}	V
	V_{OL}	CKOUT	"L" level output $I_{OL} = 4\text{ mA}$	V_{SS}	—	0.4	V
Output impedance	Z_o	CKOUT	16.6 MHz to 134 MHz	—	45	—	Ω
Input capacitance	C_{IN}	CKIN, ENS, FREQ0, FREQ1, XPD	$T_a = +25\text{ }^\circ\text{C}$, $V_{DD} = V_I = 0.0\text{ V}$, $f = 1\text{ MHz}$	—	—	16	pF
Load capacitance	C_L	CKOUT	16.6 MHz to 67 MHz	—	—	15	pF
			67 MHz to 100 MHz	—	—	10	
			100 MHz to 134 MHz	—	—	7	
Input Pull-up resistance	R_{PUE}	FREQ0	$V_{IL} = 0.0\text{ V}$	25	50	200	k Ω
	R_{PUP}	XPD		500	800	1200	
Power supply current	I_{CC}	V_{DD}	No load capacitance at 24 MHz output	—	4.0	6.0	mA
Power down current	I_{pd}	V_{DD}	Input clock stopping	—	10	—	μA

• AC Characteristics

($T_a = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$, $V_{DD} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{SS} = 0.0\text{ V}$)

Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
Input frequency	f_{in}	CKIN	—	16.6	—	134	MHz
Output frequency	f_{OUT}	CKOUT	—	16.6	—	134	MHz
Output slew rate	SR	CKOUT	Load capacitance 15 pF 0.4 V to 2.4 V	0.4	—	4.0	V/ns
Output clock duty cycle	t_{DCC}	CKOUT	1.5 V	40	—	60	%
Modulation frequency (Number of input clocks per modulation)	f_{MOD} (n_{MOD})	CKOUT	FREQ[1 : 0] = (00)	$f_{in}/2640$ (2640)	$f_{in}/2280$ (2280)	$f_{in}/1920$ (1920)	kHz (clks)
			FREQ[1 : 0] = (10)	$f_{in}/4400$ (4400)	$f_{in}/3800$ (3800)	$f_{in}/3200$ (3200)	
			FREQ[1 : 0] = (11)	$f_{in}/5280$ (5280)	$f_{in}/4560$ (4560)	$f_{in}/3840$ (3840)	
			FREQ[1 : 0] = (01)	$f_{in}/8800$ (8800)	$f_{in}/7600$ (7600)	$f_{in}/6400$ (6400)	

(Continued)

MB88153A

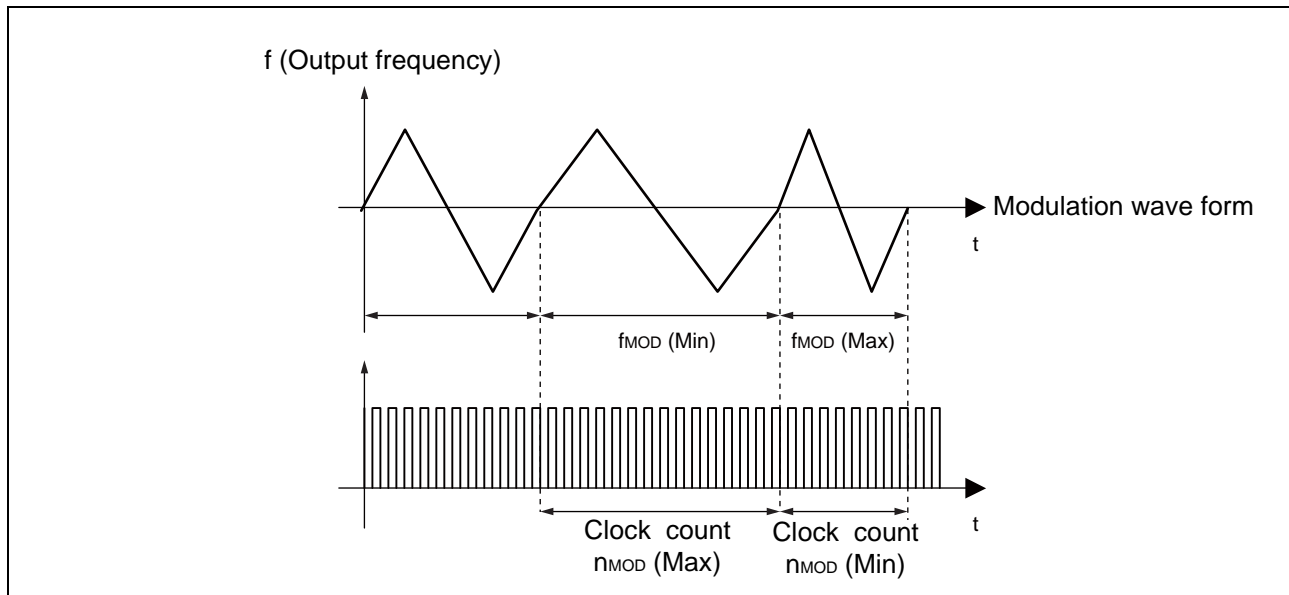
(Continued)

($T_a = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, $V_{DD} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{SS} = 0.0\text{ V}$)

Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
Lock-up time	t_{LK}	CKOUT	16.6 MHz to 80 MHz	—	2	5	ms
			80 MHz to 134 MHz	—	3	8	
Cycle-cycle jitter	t_{JC}	CKOUT	No load capacitance, $T_a = +25\text{ }^{\circ}\text{C}$, $V_{DD} = 3.3\text{ V}$	—	—	100	ps-rms

Note : The modulation clock stabilization wait time is required after the power is turned on, the IC recovers from power saving, or after FREQ (frequency range) or ENS (modulation ON/OFF) setting is changed. For the modulation clock stabilization wait time, assign the maximum value for lock-up time.

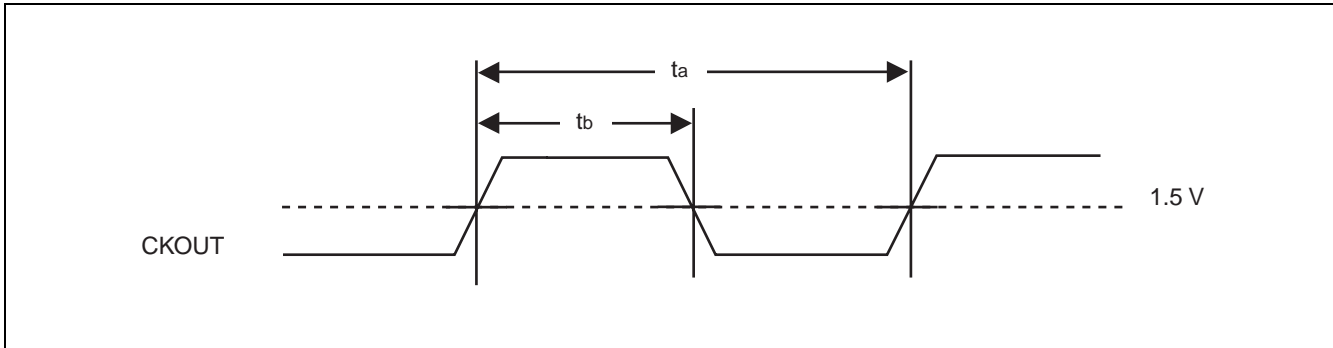
<Definition of modulation frequency and number of input clocks per modulation>



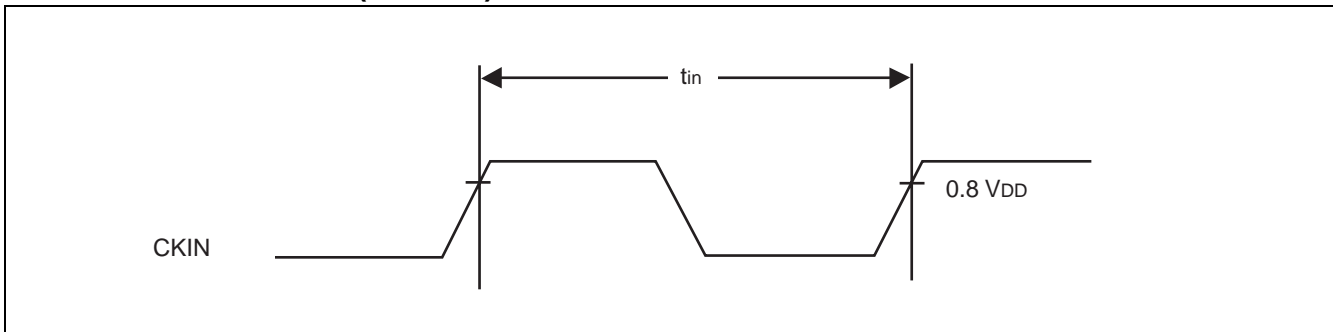
MB88153A contains the modulation period to realize the efficient EMI reduction.

The modulation period f_{MOD} depends on the input frequency and changes between f_{MOD} (Min) and f_{MOD} (Max) . Furthermore, the average value of f_{MOD} equals the typical value of the electrical characteristics.

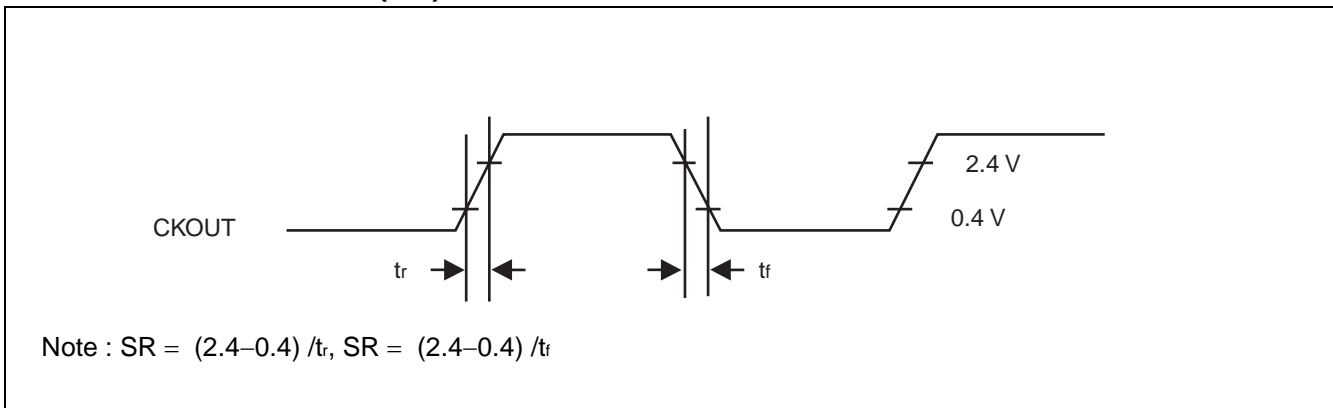
■ OUTPUT CLOCK DUTY CYCLE ($t_{DCC} = t_b/t_a$)



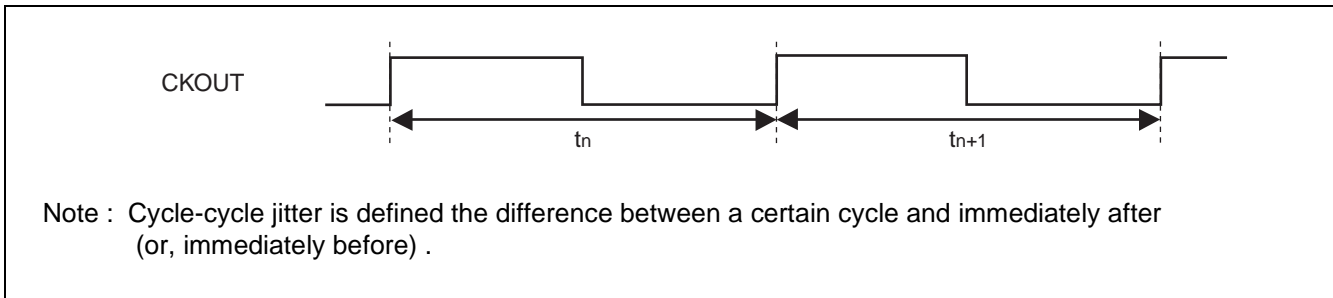
■ INPUT FREQUENCY ($f_{in} = 1/t_{in}$)



■ OUTPUT SLEW RATE (SR)

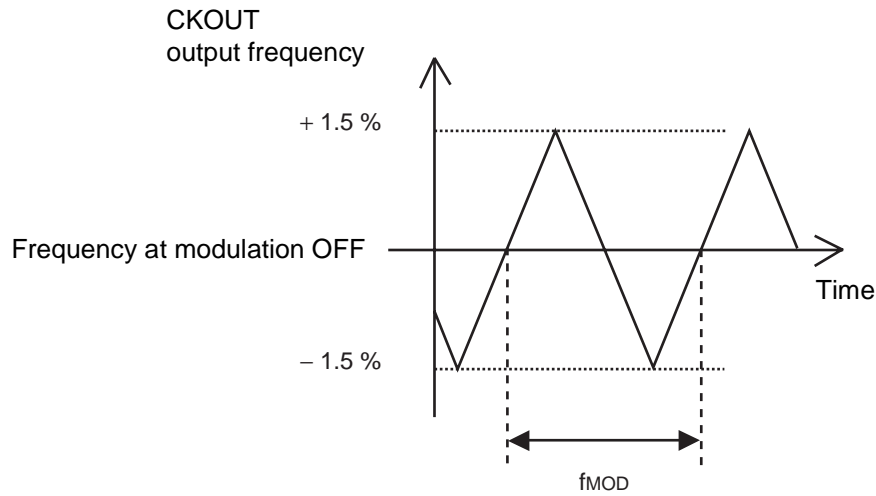


■ CYCLE-CYCLE JITTER

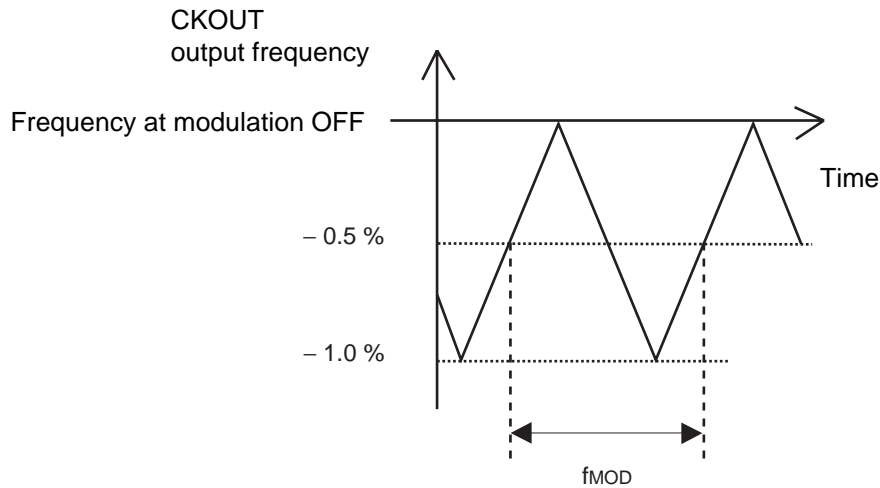


■ MODULATION WAVE FORM

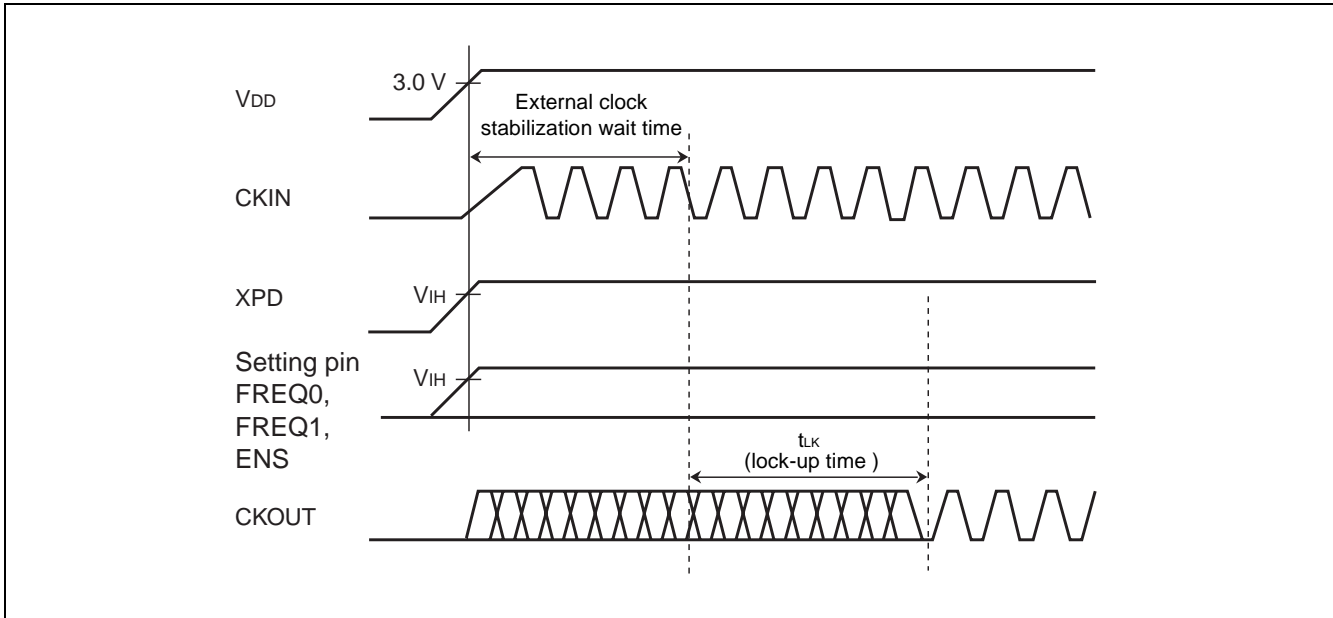
- $\pm 1.5\%$ modulation rate, Example of center spread



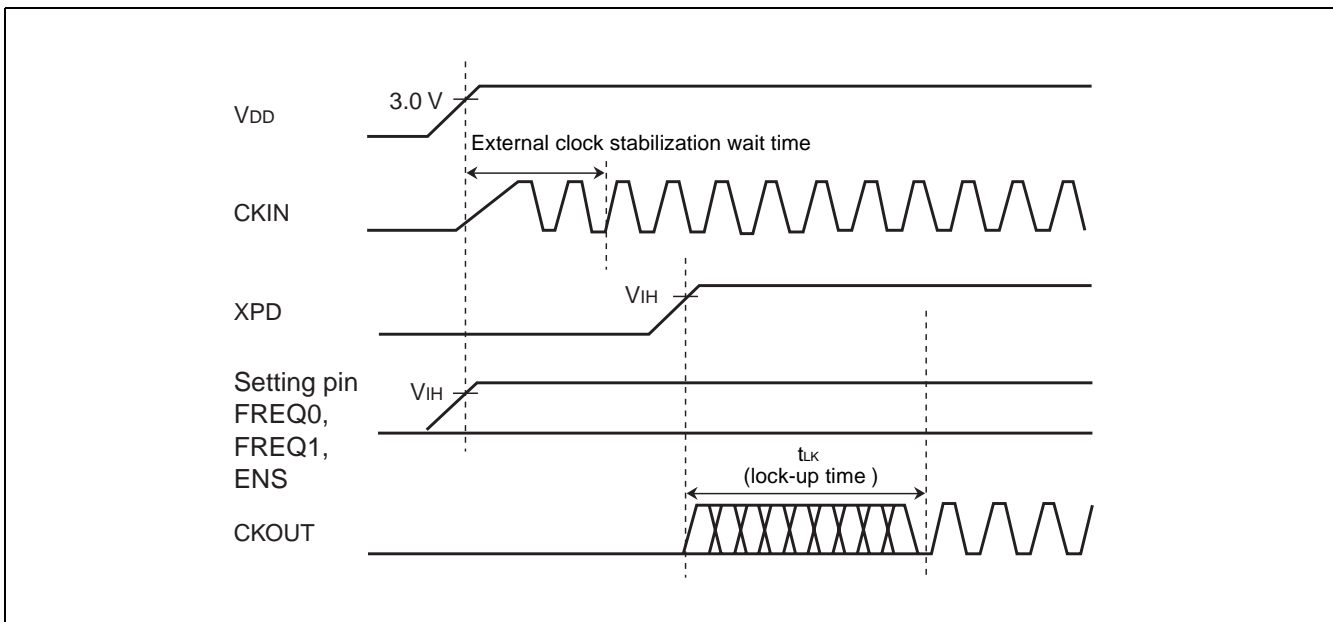
- -1.0% modulation rate, Example of down spread



LOCK-UP TIME



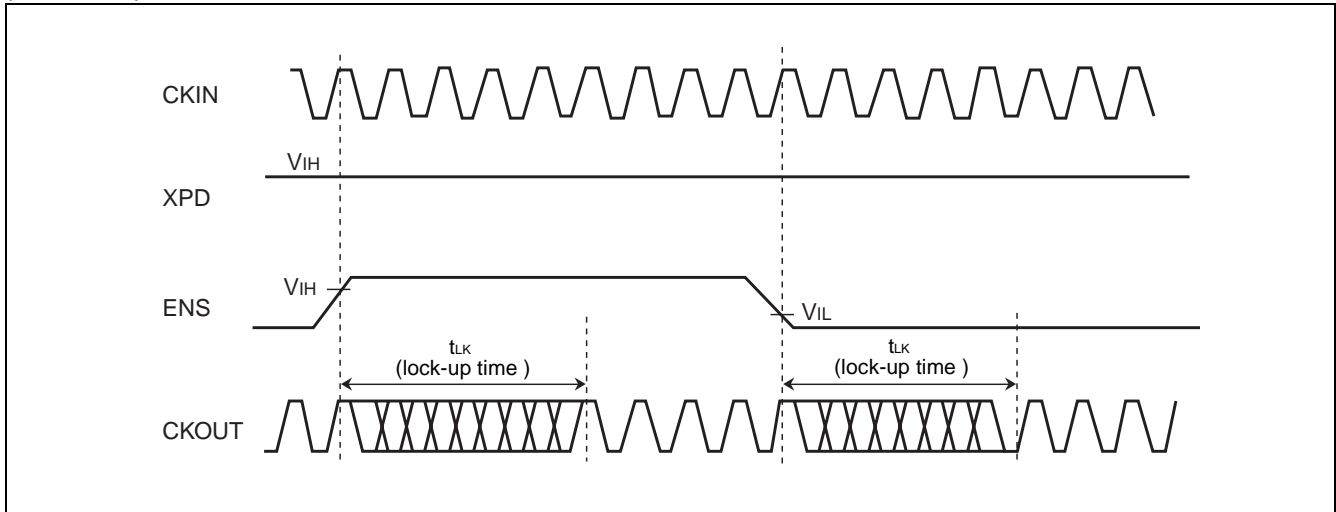
If the XPD pin is fixed at the "H" level, the maximum time after the power is turned on until the set clock signal is output from CKOUT pin is (the stabilization wait time of input clock to CKIN pin) + (the lock-up time " t_{LK} "). For the input clock stabilization time, check the characteristics of the resonator or oscillator used.



When XPD pin controls the power-down, stable clock is output from CKOUT pin after becoming XPD pin = "H" level (in the maximum after lock-Up time (t_{LK})).

(Continued)

(Continued)



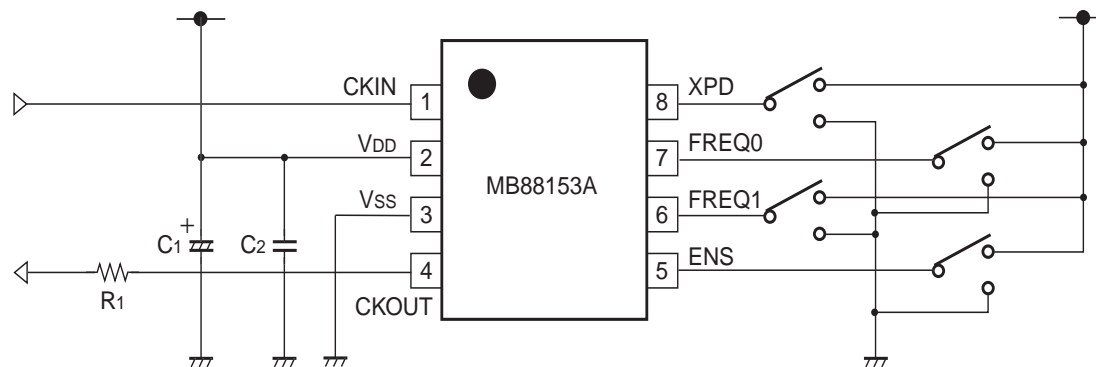
When ENS pin is controlled for enable modulation, it is necessary for the stably clock output from CKOUT pin to wait lock-up time (t_{LK}) .

Note : In the following cases, it is necessary for the stably clock output from CKOUT pin, to wait lock-up time (t_{LK}) .

- After releasing power-down
- When you change other terminal settings

Output frequency, output clock duty cycle, modulation frequency, and cycle-cycle jitter are not guaranteed until the output clock is stable. It is recommended to take procedure to release of reset after. lock-up time (t_{LK}) on the device using the modulation clock or etc.

■ INTERCONNECTION CIRCUIT EXAMPLE



C₁ : Capacitor of 10 μ F or higher

C₂ : Capacitor of approximately 0.01 μ F (connect a capacitor of good high frequency property (ex. laminated ceramic capacitor) to close to this device)

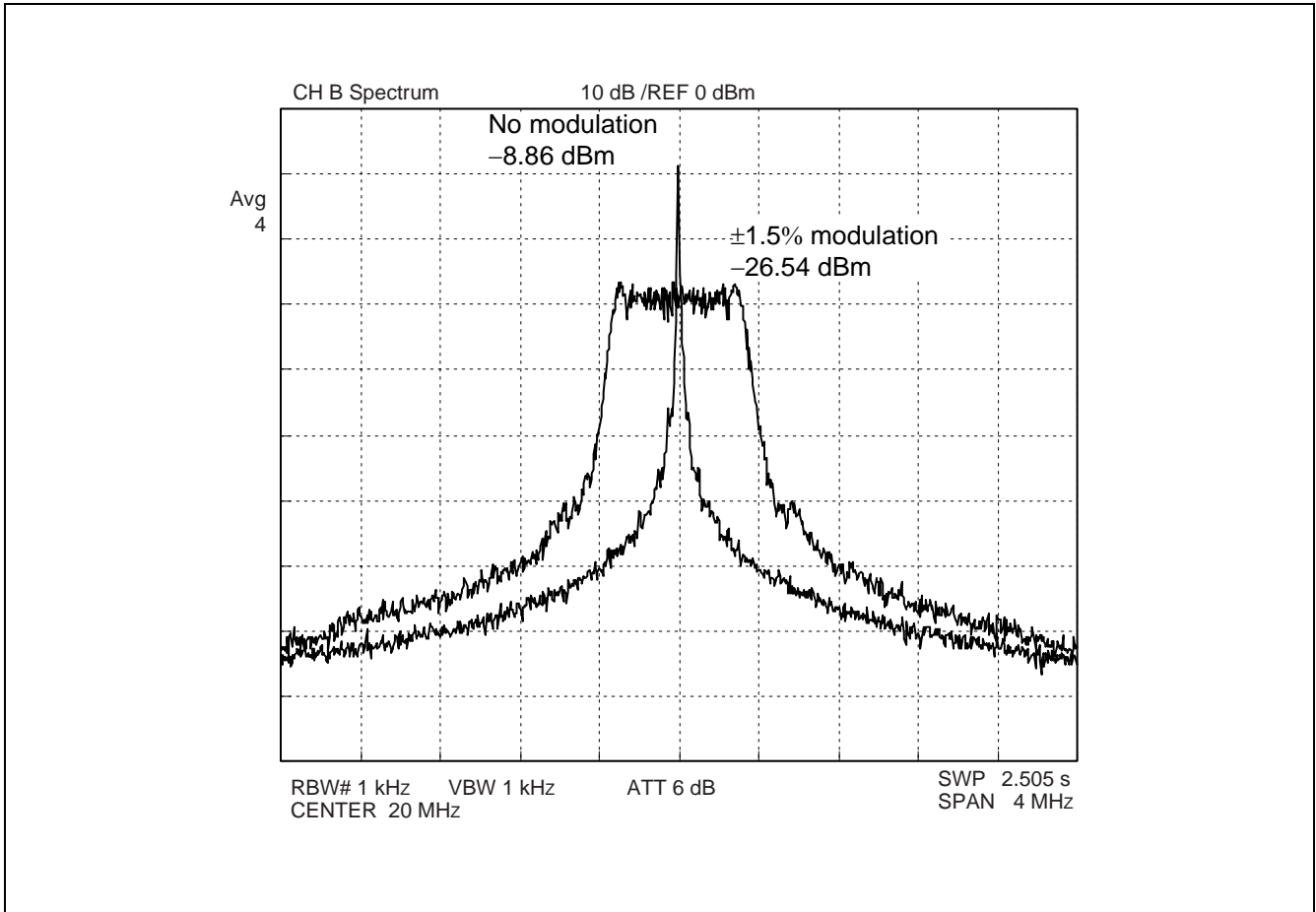
R₁ : Impedance matching resistor for a circuit on a board

■ SPECTRUM EXAMPLE CHARACTERISTICS

The condition of the examples of the characteristic is shown as follows: Input frequency = 20 MHz (Output frequency = 20 MHz), use for MB88153A-111.

Power-supply voltage = 3.3 V, None load capacity. Modulation rate = $\pm 1.5\%$ (center spread).

Spectrum analyzer HP4396B is connected with CKOUT. The result of the measurement with RBW = 1 kHz (ATT use for -6 dB) .

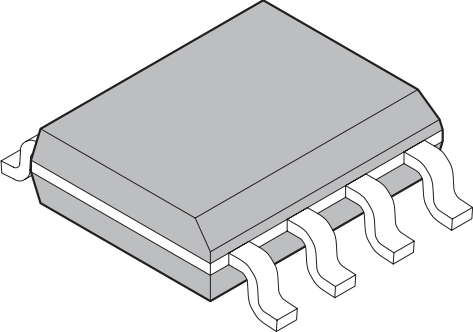


■ ORDERING INFORMATION

Part number	Modulation rate	Modulation type	Package	Remarks
MB88153APNF-G-100-JNE1	-1.0%	Down spread	8-pin plastic SOP (FPT-8P-M02)	
MB88153APNF-G-101-JNE1	-3.0%	Down spread		
MB88153APNF-G-110-JNE1	±0.5%	Center spread		
MB88153APNF-G-111-JNE1	±1.5%	Center spread		
MB88153APNF-G-100-JNEFE1	-1.0%	Down spread	8-pin plastic SOP (FPT-8P-M02)	Emboss taping (EF type)
MB88153APNF-G-101-JNEFE1	-3.0%	Down spread		
MB88153APNF-G-110-JNEFE1	±0.5%	Center spread		
MB88153APNF-G-111-JNEFE1	±1.5%	Center spread		
MB88153APNF-G-100-JNERE1	-1.0%	Down spread	8-pin plastic SOP (FPT-8P-M02)	Emboss taping (ER type)
MB88153APNF-G-101-JNERE1	-3.0%	Down spread		
MB88153APNF-G-110-JNERE1	±0.5%	Center spread		
MB88153APNF-G-111-JNERE1	±1.5%	Center spread		

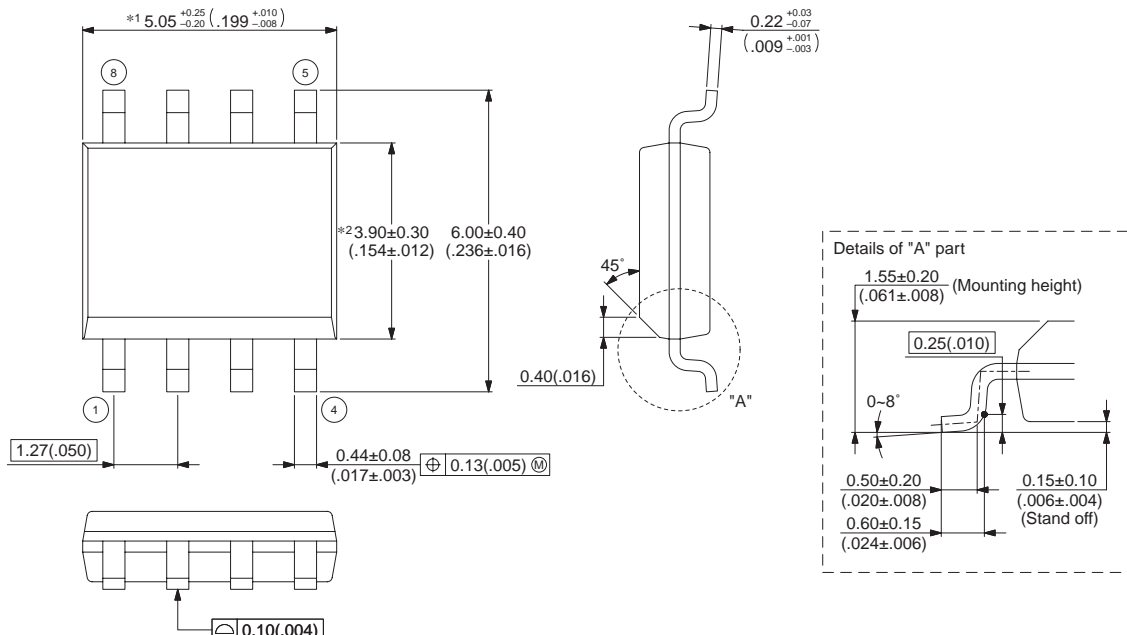
MB88153A

PACKAGE DIMENSION

 <p>8-pin plastic SOP</p> <p>(FPT-8P-M02)</p>	Lead pitch	1.27 mm
	Package width × package length	3.9 × 5.05 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.75 mm MAX
	Weight	0.06 g

8-pin plastic SOP
(FPT-8P-M02)

Note 1) *1 : These dimensions include resin protrusion.
 Note 2) *2 : These dimensions do not include resin protrusion.
 Note 3) Pins width and pins thickness include plating thickness.
 Note 4) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
 Note: The values in parentheses are reference values.

© 2002 FUJITSU LIMITED F08004S-c-4-7

Please confirm the latest Package dimension by following URL.
<http://edevice.fujitsu.com/package/en-search/>

MEMO

MEMO



MEMO

FUJITSU MICROELECTRONICS LIMITED

Shinjuku Dai-Ichi Seimei Bldg. 7-1, Nishishinjuku 2-chome, Shinjuku-ku,
Tokyo 163-0722, Japan Tel: +81-3-5322-3347 Fax: +81-3-5322-3387
<http://jp.fujitsu.com/fml/en/>

For further information please contact:

North and South America

FUJITSU MICROELECTRONICS AMERICA, INC.
1250 E. Arques Avenue, M/S 333
Sunnyvale, CA 94085-5401, U.S.A.
Tel: +1-408-737-5600 Fax: +1-408-737-5999
<http://www.fma.fujitsu.com/>

Europe

FUJITSU MICROELECTRONICS EUROPE GmbH
Pittlerstrasse 47, 63225 Langen,
Germany
Tel: +49-6103-690-0 Fax: +49-6103-690-122
<http://emea.fujitsu.com/microelectronics/>

Korea

FUJITSU MICROELECTRONICS KOREA LTD.
206 KOSMO TOWER, 1002 Daechi-Dong,
Kangnam-Gu, Seoul 135-280
Korea
Tel: +82-2-3484-7100 Fax: +82-2-3484-7111
<http://www.fmk.fujitsu.com/>

Asia Pacific

FUJITSU MICROELECTRONICS ASIA PTE LTD.
151 Lorong Chuan, #05-08 New Tech Park,
Singapore 556741
Tel: +65-6281-0770 Fax: +65-6281-0220
<http://www.fujitsu.com/sg/services/micro/semiconductor/>

FUJITSU MICROELECTRONICS SHANGHAI CO., LTD.
Rm.3102, Bund Center, No.222 Yan An Road(E),
Shanghai 200002, China
Tel: +86-21-6335-1560 Fax: +86-21-6335-1605
<http://cn.fujitsu.com/fmc/>

FUJITSU MICROELECTRONICS PACIFIC ASIA LTD.
10/F., World Commerce Centre, 11 Canton Road
Tsimshatsui, Kowloon
Hong Kong
Tel: +852-2377-0226 Fax: +852-2376-3269
<http://cn.fujitsu.com/fmc/tw>

All Rights Reserved.

The contents of this document are subject to change without notice.

Customers are advised to consult with sales representatives before ordering.

The information, such as descriptions of function and application circuit examples, in this document are presented solely for the purpose of reference to show examples of operations and uses of FUJITSU MICROELECTRONICS device; FUJITSU MICROELECTRONICS does not warrant proper operation of the device with respect to use based on such information. When you develop equipment incorporating the device based on such information, you must assume any responsibility arising out of such use of the information.

FUJITSU MICROELECTRONICS assumes no liability for any damages whatsoever arising out of the use of the information.

Any information in this document, including descriptions of function and schematic diagrams, shall not be construed as license of the use or exercise of any intellectual property right, such as patent right or copyright, or any other right of FUJITSU MICROELECTRONICS or any third party or does FUJITSU MICROELECTRONICS warrant non-infringement of any third-party's intellectual property right or other right by using such information. FUJITSU MICROELECTRONICS assumes no liability for any infringement of the intellectual property rights or other rights of third parties which would result from the use of information contained herein.

The products described in this document are designed, developed and manufactured as contemplated for general use, including without limitation, ordinary industrial use, general office use, personal use, and household use, but are not designed, developed and manufactured as contemplated (1) for use accompanying fatal risks or dangers that, unless extremely high safety is secured, could have a serious effect to the public, and could lead directly to death, personal injury, severe physical damage or other loss (i.e., nuclear reaction control in nuclear facility, aircraft flight control, air traffic control, mass transport control, medical life support system, missile launch control in weapon system), or (2) for use requiring extremely high reliability (i.e., submersible repeater and artificial satellite).

Please note that FUJITSU MICROELECTRONICS will not be liable against you and/or any third party for any claims or damages arising in connection with above-mentioned uses of the products.

Any semiconductor devices have an inherent chance of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

Exportation/release of any products described in this document may require necessary procedures in accordance with the regulations of the Foreign Exchange and Foreign Trade Control Law of Japan and/or US export control laws.

The company names and brand names herein are the trademarks or registered trademarks of their respective owners.